AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning on page 1, line 5, with the following amended paragraph:

This application ~~is based on the earlier~~ claims priority under the Paris Convention of Japanese patent applications No. 11-304683 (filed on October 26, 1999) and No. 2000-308262 (filed on October 6, 2000), ~~the priority thereof under the Paris Convention is claimed. The entire disclosures thereof~~ which are hereby incorporated herein by reference ~~thereto~~.

Please replace the paragraph beginning on page 1, line 11, with the following amended paragraph:

This invention relates ~~generally~~ to an active matrix liquid crystal display device, particularly, to an active matrix substrate and a manufacturing method therefor. More particularly, it relates to a channel protection active matrix substrate in which a gate electrode, a drain electrode and a pixel electrode are isolated ~~from layer to layer~~ between each layer ~~and~~ with the pixel electrode ~~is~~ formed as the topmost layer, and a manufacturing method therefor.

Please replace the paragraph beginning on page 1, line 20, with the following amended paragraph:

An active matrix liquid crystal display device, ~~employing~~ with an active element, such as a thin-film transistor, which is thin in thickness and lightweight, ~~and~~ is utilized as a flat panel high picture quality display ~~of a high picture quality~~. ~~For a~~ A liquid crystal display ~~device,~~ has a vertical electrical field system (typically formed as a twisted nematic or TN

system) in which a liquid crystal is sandwiched between two substrates carrying transparent electrodes ~~and is~~ driven by a voltage applied across these electrodes, and a lateral (in-plane) electrical field system in which a liquid crystal layer is sandwiched between and driven by comb-shaped pixel electrodes in which the voltage is applied generally along the plane of the electrodes. In both systems, ~~researches are~~ research has been conducted towards simplifying the production process of an active matrix substrate for lowering the production cost. On the other hand, the opening ratio needs to be raised for achieving a high-grade picture. To this end, such a method is used in which a transparent electrode (indium tin oxide or ITO) layer and a drain layer are isolated on the layer basis and the transparent electrode layer is formed as a topmost layer.

Please replace the paragraph beginning on page 2, line 24, with the following amended paragraph:

~~As a~~ A manufacturing method in which the transparent electrode layer is formed as the topmost layer to simplify and diminish the number of steps of the production process, which is a technique shown in JP Patent Kokai JP-A-10-68971, is explained with reference to Fig.62, which is a cross-sectional view for schematically showing the processes of the manufacturing method for an active matrix substrate for use in a TN system liquid crystal display device.

Please replace the paragraph beginning on page 2, line 7, with the following amended paragraph:

In general, the active matrix substrate of the TN system is comprised of a gate wiring lines and a drain wiring lines extending in a direction perpendicular to each other, a pixel electrode defined in an area surrounded by these wiring lines, and a thin-film transistor (TFT)

formed in the vicinity of the intersection of the two wiring lines. On the surface of the TFT is formed a channel protection film for assuring the performance. On the TFT and the pixel electrode on the active matrix substrate, ~~there is formed~~ an orientation film for orienting the liquid crystal in the pre-set direction is formed. A liquid crystal is sealed between the active matrix substrate and a counter substrate carrying a color filter, a common electrode and an orientation film to complete the liquid crystal device.

Please replace the paragraph beginning on page 4, line 16, with the following amended paragraph:

Then, a contact hole for exposing a source/drain electrode areas is formed, using a fourth photomask, ITO film 108 which is deposited on the entire surface of the substrate 101, and the ITO film 108 in the preset area is removed, using a fifth photomask, to form a pixel electrode connected to the source electrode, ~~to complete~~ which completes the production of the active matrix substrate, as shown in Fig.62(d).

Please replace the paragraph beginning on page 4, line 25, with the following amended paragraph:

In this conventional active matrix substrate, the ITO film 108 is not provided on the same layer as the source/drain electrode layer 106, and the film is insulated and separated by the second passivation film 107. So, for insulation and isolation of the ITO film108 from the drain electrode layer 106, ~~these are not in need of being~~ they do not need to be separated from each other laterally relative to a normal line drawn to the active matrix substrate, and hence ~~these can be made to approach extremely closely~~ they can be made extremely close to or even overlap with each other. Thus, the black matrix for shielding the uncontrolled backlight

~~straying~~ which strays from a gap produced when the ITO film 108 and the source/drain electrode layer 106 are separated from each other can be diminished to elevate the opening ratio. This accounts for ~~insuation~~ insulation and separation of the ITO film 108 and the drain electrode layer 106 from each other by the second passivation film 107.

Please replace the paragraph beginning on page 5, line 15, with the following amended paragraph:

It is noted that the ITO film 108 is insulated and separated from each other by the passivation film 107. In this conventional method for preparing the active matrix substrate, the active matrix substrate can be produced by five masks ~~as~~ with the transparent electrode layer ~~is~~ formed as the uppermost layer.

Please replace the paragraph beginning on page 5, line 21, with the following amended paragraph:

Various problems have been encountered in the course of ~~investigations~~ investigation toward the present invention.

Please replace the paragraph beginning on page 5, line 23, with the following amended paragraph:

In the method, shown in the above-mentioned Publication, the gate electrode, drain electrode and the pixel electrode of ITO film are isolated on the layer basis by five masks to produce an active matrix substrate carrying a topmost ITO film. ~~There~~ A problem is, however, presented ~~a problem~~ that, since the second passivation film 107, a-Si layer 104 and the gate insulating film 103 are etched in a lump at the process step of Fig.62(c), the lateral

surface of the a-Si layer 104 is exposed without being covered by the second passivation film 107.

Please replace the paragraph beginning on page 5, line 23, with the following amended paragraph:

If the ITO film 108 contacts the lateral surface of the a-Si layer 104, not covered by the passivation film, then the metal as a constituting component of the ITO film 108 is diffused as impurity into the inside of the a-Si layer 104, thereby appreciably deteriorating the performance of the thin-film transistor. For ~~evading~~ avoidance of this problem, the passivation film can again be deposited after the step of Fig.62(c) and before the step of Fig.62(d) to protect the lateral side of the a-Si layer 104 with the passivation film. There is, however, ~~raised~~ a problem raised that deposition of the passivation film a second time increases the number of process steps.

Please replace the paragraph beginning on page 7, line 2, with the following amended paragraph:

In general, there is much to be desired in the conventional art and ~~it is desired to provide~~ a novel device and method is needed.

Please replace the paragraph beginning on page 7, line 17, with the following amended paragraph:

Other aspects and objects ~~will become apparent by~~ are described in the entire disclosure.

Please replace the paragraph beginning on page 21, line 4, with the following amended paragraph:

In an active matrix substrate according to a preferred embodiment of the present invention, the gate electrode layer, gate insulating film and the a-Si layer are processed to the same shape to form a gate electrode layer (102 of Fig.6) and a TFT area, and a drain electrode layer (106 of Fig.6) is formed on a first passivation film (105 of Fig.6) as an overlying layer. In a second passivation film (107 of Fig.6) formed as an overlying layer of the drain electrode layer 106, ~~there are provided with~~ a first opening (through-hole) ~~passing~~ passes through the first and second passivation films and ~~with~~ a second opening ~~passing~~ passes through the second passivation film, and a connection wiring layer is formed by ITO of the uppermost layer (108 of Fig.6), ~~whilst~~ while a storage capacitance unit is provided in a pixel electrode for sandwiching the first and second passivation films in ~~cooperation~~ coordination with an electrode layer formed as a co-layer as the gate electrode.

Please replace the paragraph beginning on page 21, line 20, with the following amended paragraph:

An embodiment of the present invention will be explained ~~for further illustrating~~ to illustrate the present invention in detail.

Please replace the paragraph beginning on page 24, line 18, with the following amended paragraph:

The layered structure, made up of a gate electrode layer 102, a gate insulating film 103 and an a-Si layer 104, formed in a substantially overlapping fashion, ~~correspond~~ corresponds to the gate bus lines 1 and to the gate electrode 2. The drain electrode layer 106 corresponds

to the drain bus lines 4.

Please replace the paragraph beginning on page 24, line 23, with the following amended paragraph:

Moreover, the active matrix substrate of the present embodiment includes plural slits 8, as shown in Fig.5. the slits 8 are provided in pairs above the gate bus lines 1 on both sides of the drain bus lines 4 at a location where the drain bus lines 4 intersects the gate bus lines 1. Stated differently, the slits 8 are formed above the gate bus lines 1 intermediate between one end of the pixel electrode 11, extending to above the gate electrode layer 102 for defining the storage capacitor 108 between it and the gate electrode layer 102, and the drain bus lines 4. These slits 8 are openings formed in the first and second passivation films 105, 107. The gate insulating film 103 and the a-Si layer 104 are removed in a location of the layered product where these slits 8 are formed. The gate bus lines 1 is of a three-layered structure comprised of the gate electrode layer 102, gate insulating film 103 and the a-Si layer 104 where the gate bus lines 1 intersect the drain bus lines 4. The paired slits 8, formed on both outer sides of the drain bus lines 4, serve to remove the gate insulating film 103 and the a-Si layer 104 so as to fractionate the a-Si layer 104 into plural shorter domains isolated from one another. In the absence of the slits 8, ~~there are produced~~ parasitic transistors ~~to~~ are produced which cause a malfunction. By providing the slits 8, no parasitic transistors are produced ~~to prevent~~ which prevent the malfunction.

Please replace the paragraph beginning on page 26, line 16, with the following amended paragraph:

Then, a first passivation film 105, such as SiNx, is formed by e.g., a plasma CVD method, ~~whilst~~ while an underlying layer of metals, such as Ti, Cr or Mo, which later becomes the drain electrode layer 106, and a layered film of Al etc, are formed by e.g., a plasma CVD method, on the entire surface of a transparent insulating substrate 101. Preferably, the film thickness of the first passivation film 105 is approximately 0.2 μm, ~~whilst~~ while the film thicknesses of the underlying layer of Ti and Al, as the drain electrode layer 106, are approximately 50 nm and 0.2 μm, respectively.

Please replace the paragraph beginning on page 27, line 1, with the following amended paragraph:

After the film formation, a resist pattern is formed to overlie a drain bus line 4, using a second mask, as shown in Figs.3 and 6(b), ~~whilst~~ while an unneeded metal layer (part) is removed by dry etching, to form a dry buss line 4.

Please replace the paragraph beginning on page 30, line 25, with the following amended paragraph:

In this manner, ~~<the active matrix substrate>~~ the active matrix substrate of the present embodiment includes a layered structure (product) of the gate electrode layer 102, gate insulating film 103 and the a-Si layer 104, deposited in a substantially stacked fashion on the transparent insulating substrate 101. And it is produced by forming the first passivation film 105 on the transparent insulating substrate 101 for overlying the layered structure, forming the drain electrode layer 106 on the first passivation film 105, forming the second passivation film 107 on the first passivation film 105 for overlying the drain electrode layer 106, forming the source opening 7 and the drain opening 6 in the first and second passivation films 105,

107 for exposing the a-Si layer 104, forming the source electrode 10 on the second passivation film 107 so as to be electrically connected to the other end of the a-Si layer 104 through the source opening 7, and by forming the pixel electrodes 11 on the second passivation film 107 so that one ends thereof are formed integrally with the source electrode 10. So, there can be realized an active matrix substrate in which the gate electrode 2, drain electrode 9 and the pixel electrode 11 are separated from one another on the layer basis, and in which the surface and sidewall sections of the a-Si layer 104 of the layered structure are covered by the first and second passivation films 105, 107. This prevents the ITO film from contacting the lateral side of the a-Si layer 104 while improving the long-term reliability of the thin film transistor and active matrix substrate into which this thin film transistor is realized. Moreover, if the active matrix substrate is arranged as a liquid crystal display device, then it is possible to prevent the a-Si layer from contacting the liquid crystal material.

Please replace the paragraph beginning on page 32, line 5, with the following amended paragraph:

In addition, in the manufacturing method for the active matrix substrate of the present embodiment, a layered structure (product) of the gate electrode layer 102, gate insulating film 103 and the a-Si layer 104 is formed and is covered by the first passivation film 105, the drain electrode layer 106 is deposited on the first passivation film 105, the second passivation film 107 is deposited to cover the drain electrode layer 106 and the first passivation film 105, the source opening 7 and the drain opening 6 for exposing the a-Si layer 104 are formed in the first and second passivation films 105, 107, the source electrode 10 electrically connected to the opposite end of the a-Si layer 104 through the source opening 7 is provided on the second passivation film 107 and the pixel electrodes 11 having one of the ends connected integrally

to the source electrode 10 are provided on the second passivation film 107.

Please replace the paragraph beginning on page 32, line 20, with the following amended paragraph:

In the manufacturing method for the active matrix substrate of the present embodiment, there may be formed a channel protection type active matrix substrate in which the gate electrode 2, drain electrode 9 and the pixel electrode 11 are separated on the layer basis by respective insulating films, ~~whilst~~ while the surface and the sidewall of the a-Si layer 104 are completely covered by the first passivation film 105 and the second passivation film 107 by merely four masks. So, the production method may be simplified by at least one PR process as compared to the conventional manufacturing process.

Please replace the paragraph beginning on page 33, line 11, with the following amended paragraph:

The reason the gate terminal 14, drain terminal 15 and the storage capacitor 18 are configured as shown is that the first passivation film 105, second passivation film 107, the a-Si layer 104 and the gate insulating film 103 have been removed in the process of Fig.6d, with the ITO film 108 as an etching mask. The gate terminal unit 104 is formed by an exposed portion of the gate electrode layer 102, ~~whilst~~ while the drain terminal 15 is comprised of the ITO film 108 layered on the drain electrode layer 106. The storage capacitor 18 is comprised of the first and second passivation films 105, 107 sandwiched between the gate electrode layer 102 and the ITO film 108 operating as a storage capacity

electrode. On the other hand, the a-Si layer 104 is separated on the TFT basis by a slit 8 provided in the gate bus line 1. It is noted that a common potential furnishing terminal 19 for furnishing the common potential to a common electrode 13 of the liquid crystal may be manufactured to be of the same structure as the gate terminal 14 or the drain terminal 15.

Please replace the paragraph beginning on page 36, line 7, with the following amended paragraph:

As for other methods for planarization, there ~~are such~~ is a method in which film forming conditions, such as film forming rate or temperature, for SiO_2 of the second passivation film 107, to form a film of a coarse film quality, and there is a method in which dual coarse SiO_2 films are formed on a dense SiO_2 film.

Please replace the paragraph beginning on page 36, line 24, with the following amended paragraph:

Then, using a third mask, a source opening 7 in the upper portion of the a-Si layer 104, and a drain opening 6 are formed, ~~whilst~~ while a pre-set contact hole 5 is formed in each of the gate bus line 1 and the drain bus line 4, as shown in Fig.10(c). For realizing ohmic connection to the a-Si layer 104, phosphorous is diffused in a PH_3 plasma atmosphere into the a-Si layer 104 to deposit an n^+ layer as its surface layer. The ITO film 108, which later becomes the pixel electrode 11, is then deposited on the entire surface of the substrate 101 and, using a fourth mask, the source electrode 10 is connected to the pixel electrode 11, while the drain electrode 9 is connected to the drain bus line 4, as shown in Fig.10(d).

Please replace the paragraph beginning on page 41, line 4, with the following amended paragraph:

The capacitance electrode layer 110 and the pixel electrodes 11 are interconnected via ~~an~~; an opening for storage capacitor 12. The a-Si layer 104 and the gate insulating film 103 are etched off in the present embodiment at the time of etching to separate the a-Si layer 104 on the layer basis.

Please replace the paragraph beginning on page 41, line 21, with the following amended paragraph:

In the above-described manufacturing method for the active matrix substrate of the present embodiment, the gate electrode layer 102, drain electrode layer 106 and the pixel electrode 11 are separated ~~from layer to layer~~ between each layer solely by four masks to ~~realize~~ form a channel protection type active matrix substrate in which the ITO film 108 is mounted as an uppermost layer, thus simplifying the manufacturing process at least by one PR as compared to the conventional manufacturing process.

Please replace the paragraph beginning on page 42, line 4, with the following amended paragraph:

Moreover, the capacitance electrode layer 110 is formed simultaneously with the step of forming the drain electrode layer 106, ~~whilst~~ while the opening for storage capacity 12 interconnecting the capacitance electrode layer 110 and the pixel electrodes 11 is formed simultaneously with the step of forming the source opening 7 and the drain opening ~~6, the~~ 6. The storage capacitance of the storage capacitor 18 can be larger than in the first embodiment, subject to change in the mask pattern, without increasing the number of masks.

Please replace the paragraph beginning on page 52, line 3, with the following amended paragraph:

The first passivation film 105 of, for example, SiNx, is deposited on the entire surface of the transparent insulating substrate 101, ~~whilst~~ while a layered film comprised of underlying metal such as Ti, Cr or Mo, which later serves as the drain electrode layer 106, and Al, is formed thereon by e.g., the sputtering method. The first passivation film 105 is formed on the transparent insulating substrate 101 for covering the gate electrode layer 102 in the gate bus lines 1 and for covering the layered product of the a-Si layer 104, gate insulating film 103 and the gate electrode layer 102 in the gate electrode 2.

Please replace the paragraph beginning on page 55, line 5, with the following amended paragraph:

If the manufacturing method of the present embodiment is used, then the structure of the contact portions A to C, shown in the circuit diagram of Fig.23, is as shown in Fig.34. The protective bus lines 23, formed in parallel with the gate bus lines 1, are deposited on the transparent insulating substrate 101 simultaneously with and as the same layer as the gate bus lines 1, that is simultaneously with and as the same layer as the gate electrode layer 102, such that the protective bus lines 23 formed parallel to the drain bus lines 4 are formed simultaneously as and in the same layer as the drain bus lines 4, that is as the drain electrode layer 106. These protective bus lines 23 are connected in common at a circuit contact point A and connected to protective bus lines 23. Since these protective bus lines 23 are formed in respective different layers, there is provided a configuration for interconnecting the protective bus lines 23. The protective bus line 23, formed parallel to the gate bus lines 1, is covered by the first and second passivation films 105, 107 except the openings, ~~whilst~~ while the

protective bus line 23, formed parallel to the drain bus lines 4, is covered by the second passivation film 107, except the openings. These protective bus lines 23 are interconnected via these openings by the ITO film 108 deposited on the second passivation film 107. For the circuit contacts B and C, there is employed an interconnecting structure by the ITO film 108. That is, such a configuration is used at wiring nodes B and C. Thus the connection portions in the active matrix substrate used for interconnecting the wiring of the same layer as the gate electrode layer 102 and the wiring of the same layer as the drain electrode layer 106 is made via the ITO film 108 as is shown in Fig.34.

Please replace the paragraph beginning on page 56, line 21, with the following amended paragraph:

Moreover, in the present embodiment, the gate electrode layer 102 operating as the gate bus lines 1 is covered by the first and second passivation films 105, 107, ~~whilst~~ while there is provided no a-Si layer nor the gate insulating film, which are provided in the first to the fourth embodiments. So, the storage capacitance of the storage capacitor 18 may be increased by formation on the second passivation film 107 with an extension over the gate bus lines 1.

Please replace the paragraph beginning on page 61, line 18, with the following amended paragraph:

Thus, with the present embodiment of the manufacturing method for the active matrix substrate, as in the previous embodiments, the gate electrode layer 102, drain electrode layer 106 and the pixel electrodes 11 are separated, from layer to layer, by only four masks, thus realizing a channel protection type active matrix substrate having the ITO film 108 as the

topmost layer, thus simplifying the manufacturing process at least by one PR as compared to the conventional process. Moreover, since the capacitance electrode layer 110 is formed simultaneously in the production process of the drain electrode layer 106, ~~whilst~~ while the opening for storage capacitance 12 interconnecting the capacitance electrode layer 110 and the pixel electrodes 11 is formed simultaneously in the same production step as the source opening 7 and the drain opening 6, the storage capacitance in the storage capacitor 18 can be larger than that in the fifth embodiment merely by changing the mask pattern without increasing the number of masks.

Please replace the paragraph beginning on page 62, line 10, with the following amended paragraph:

Moreover, in the present embodiment, as in the fifth embodiment, the ITO film 108 can be formed by the same step not only in the drain terminals 15 but also in the gate terminals 14. That is, the gate terminals 14 can be realized as in the manufacturing process shown in Fig.31, ~~whilst~~ while the drain terminals 15 can be realized as in the manufacturing process shown in Fig.32. This enables interconnection of different wiring layers to the ITO film 108 and hence the interconnection of the protective element 22 to the respective gate terminals 14 and drain terminals 15.

Please replace the paragraph beginning on page 63, line 1, with the following amended paragraph:

Referring to Figs.41 to 55, an active matrix substrate according to a seventh embodiment of the present invention and a manufacturing method therefor, are hereinafter explained. Figs.41 to 46 are top plan views schematically showing the manufacturing process

for the active matrix substrate according to the seventh embodiment of the present invention and particularly showing a sole pixel. Figs.47 and 48 are cross-sectional views for illustrating the manufacturing process of the active matrix substrate according to the seventh embodiment of the present invention and specifically showing the cross-section taken along line K-K' in Figs.41 to 46. Figs.49 and 50 are cross-sectional views schematically showing the manufacturing process for the gate terminal unit, ~~whilst~~ while Figs.51 and 52 are cross-sectional views schematically showing the manufacturing process for the drain terminal unit nd Figs.53, 54 are cross-sectional views schematically showing the manufacturing process for the gate storage capacitor unit, taken along line L-L' of Fig.41. Fig.55 is a cross-sectional view schematically showing the structure of the gate-drain interconnection of the active matrix substrate according to the seventh embodiment of the present invention.

Please replace the paragraph beginning on page 66, line 6, with the following amended paragraph:

The ITO film 108, which serves as the pixel electrodes 11, is deposited on the entire surface of the transparent insulating substrate 101 and, using a fourth mask, the source electrode 10, pixel electrode 11, drain electrode 9 and the drain bus line 4 are interconnected, at the same time as the capacitance electrode layer 110 and the pixel electrodes 11 are interconnected, as shown in Figs.46 and ~~48(d)~~ 48(b). This realizes the active matrix substrate of the COT structure shown in Fig.39(b).

Please replace the paragraph beginning on page 68, line 18, with the following amended paragraph:

Moreover, in the present embodiment, as in the fifth embodiment, the ITO film 108 can be formed not only in the drain terminals 15 but also in the gate terminals 14 by the same process. That is, the gate terminals 14 can be realized as in the manufacturing process shown in Fig.31, as in the fifth embodiment (see Figs.49 and 50), ~~whilst~~ while the drain terminals 15 can be realized as in the manufacturing process shown in Fig.32 (see Figs.51 and 52). This realizes connection of the different interconnection layers at the ITO film 108, as shown in Fig.34.

Please replace the paragraph beginning on page 69, line 8, with the following amended paragraph:

An active matrix substrate according to a seventh embodiment of the present invention, and a manufacturing method therefor, are now explained. The present embodiment differs from the above-described seventh embodiment in that metal as a capacitance electrode layer is deposited through a passivation film at a pre-set location on the gate bus line as in the sixth embodiment to increase the capacitance of the storage capacitor (see Figs.36 and 40 for reference ~~sake~~). In other respects, the present embodiment is similar to the above-described seventh embodiment (see Figs.53 and 54 for reference ~~sake~~).

Please replace the paragraph beginning on page 69, line 18, with the following amended paragraph:

In the present embodiment, as in the third and sixth embodiments, a capacitance electrode layer is formed simultaneously with the formation of the drain electrode layer operating as the drain bus line (see Figs.36 and 40 for reference ~~sake~~). This capacitance

electrode layer operates as a storage capacitance electrode of the storage capacitor realized between it and the gate electrode layer.

Please replace the paragraph beginning on page 69, line 25, with the following amended paragraph:

Then, the black matrix and the planarizing film then are formed on the substrate in the same manner as in the seventh embodiment (see Figs.53 and 54 for reference ~~sake~~). An opening for storage capacitance 12 is formed when forming the source opening and the drain opening in an upper portion of the a-Si layer and the contact hole in an upper portion of the drain bus line, using the third mask (see Fig.37 for reference ~~sake~~).

Please replace the paragraph beginning on page 71, line 21, with the following amended paragraph:

In the present embodiment, as in the fifth embodiment, an ITO film may be formed not only in the drain terminal 15 but also in the gate terminals by the same step. That is, the gate terminals can be produced by the manufacturing process shown in Fig.31, ~~whilst~~ while the drain terminal can be produced by the manufacturing process shown in Fig.32, as in the fifth embodiment. This enables different wiring layers to be connected at the ITO film, as shown in Fig.34, while simultaneously realizing the connection of the protective element to the gate terminals 14 and to the drain terminals 15.

Please replace the paragraph beginning on page 75, line 68, with the following amended paragraph:

Then, on the entire surface of the transparent insulating substrate 101, the gate bus lines 1, comb-shaped common electrode 13 and the first passivation film 105 of, for example, SiNx, covering the layered structure, are formed by e.g., the plasma CVD method, ~~whilst~~ while a layered film of underlying metals, such as Ti, Cr and Mo, and Al, which later servers as the drain electrode layer 106, is formed by e.g., sputtering. Then, as shown in Figs.58 and 61(b), the drain bus lines 4 and the pixel electrodes 11 are formed, using the second mask. The drain bus lines 4 are extended in a direction intersecting the gate bus lines 1 and are branched on the first passivation film 105 between the gate bus lines 1 and the common electrode 13 so as to extend to the vicinity of the gate electrode 2. The pixel electrodes 11 are comb-shaped and arranged between the plural drain bus lines 4.

Please replace the paragraph beginning on page 77, line 5, with the following amended paragraph:

Moreover, in the present embodiment, the ITO film 108 can be formed by the same process not only the drain terminals 15 but also the gate terminals 14 as in the fifth and sixth embodiments. That is, the gate terminals 14 can be formed by the manufacturing process shown in Fig.31, ~~whilst~~ while the drain terminals 15 can be formed by the manufacturing process shown in Fig.32, as in the above-described fifth and sixth embodiments. This enables different wiring layers to be connected at the ITO film, as shown in Fig.34, while simultaneously realizing the connection of the protective element to the gate terminals 14 and to the drain terminals 15.

Please replace the paragraph beginning on page 77, line 16, with the following amended paragraph:

In addition, with the active matrix substrate of the present embodiment, the gate bus lines 1 and the common electrode 13 are covered by the first passivation film 105, ~~whilst~~ while the a-Si layer 104 and the gate insulating film 103 are removed. So, the first passivation film 105 is improved in planarity in the vicinity of the common electrode 13 as compared to that in the fourth embodiment. The comb-shaped common electrode 13, formed on the first passivation film 105, thus improved in planarity, is improved further in long-term reliability. Since the entire surface of the active matrix substrate can be improved in planarity as compared to that in the fifth embodiment, it is possible to improve controllability of the orientation of the liquid crystal.